Design and Realization of Multi-Channel Digital Receivers for Active Phased Array Radar

D.Govind Rao[1], Hassen Basha[2], Renuka Prasad[3],Anant Raut[4]
Electronics and Radar Development Establishment, DRDO, Bangalore
dgrao@ lrde.drdo.in,hassenbasha@lrde.drdo.in

Abstract:

Modern Active Phased array Radars consist of thousands of transmit receive (T/R) T/R elements which are controlled using distributed digital receiver architecture. Groups of radiating T/R elements are controlled simultaneously to steer the beam and the received echo is processed in digital domain to obtain complex digital video signals.

The digital processing of the resultant signals offers great flexibility and accurate computation to form Digital Beam Forming (DBF)". An effort has been made to bring the analog system and digital system together as demanded by the state of the art Active Phased Array Radars.This requirement has been achieved by using analog and digital circuits densely packed to form Multi-Channel Analog and Digital Receiver. A hybrid design involving Multi-Channel Analog and Digital receiver design as a single compact unit being realized for Active phased array radar has been brought out in this paper.

In this paper, we are mainly considering the implementation of the multi-channel digital receiver. The multi-channel receiver will operates in various modes of operation. The calibration of each receiver will be critical for receive path as well as for transmit path. The main focus of this paper is on calibration, configuration and pattern measurement process of multi-channel receiver.

The H/w designed in small size so that it can be fixed into a active phased array radar has been brought out in this paper.

Key Words: Active Phased Array Radar, VIRETX5 FPGA, DDC, Calibration, SIMULINK, Beam Steering, Phase, Attenuation, ADC, DBF, MSTC, T/R modules.

I INTRODUCTION

The Radar receiver is an important subsystem of the Phased Array Radar which determines the system performance. The Radar receiver consists of two different domains viz. Analog Receiver and digital receiver. The main function of analog receiver is to convert high frequency signal from several GHz to low frequency signal of several MHz's to carry out this conversion. we have used super heterodyne based double down conversion method to convert low frequency signal.

The digital receiver which is an integral part of the phased array radar system, A high resolution ADC is used to convert the analog signal to digital signal and further Digital Down conversion is carried out to convert the signal to bas band. The realization of digital receiver is done using the state of the art FPGA which is high speed and high performance. The active phased array Radar consists of several hundreds of receiver channels. Each one of the receiver channel will receive the signal from the T/R Modules during receive mode of radar operation. Eight different analog Receiver and Digital receivers are combined into one group known as Multi channel Receivers.

II DESIGN APPROACH

The Multi-Channel receivers are required to process the signal from multiple receive beams. There can be N multi-channel receiver in phased array configuration. These Multi-Channel Receivers are synchronized with the common signal called Trigger signal. All the Radar Modes of operation will accompany with trigger Signal. All the receivers will receive the signal from the T/R Modules during receive mode of radar operation. Transmit and receive mode of operation will be controlled with the help of pulsed signal called PRT. The PRT generation is controlled with the help of time synchronous trigger signal .The eight channel receivers will process the signal. The eight channels down converted digital data will be multiplexed. This multiplexed data is transmitted over high speed serial optical to digital beam former unit. Digital Beam former will process and form multiple receives beams for further processing. Each Eight channel receiver has a dedicated duplex optical communication channel.

The digital receiver parameters can be configured using control received from the Digital Beam Former as a message. An FIR filter is designed are selected for required range resolution of radar operation. There are two low pass filters in the designed architecture which can be configured using the command for Type 1 OR Type 2 bandwidth. With the help of Mux we can select either one of the filters online radar mode of operation. The DDS generation is synchronized with actual radar operation. The Figure 1 shows the Multi-channel architecture in the phased array Radar.

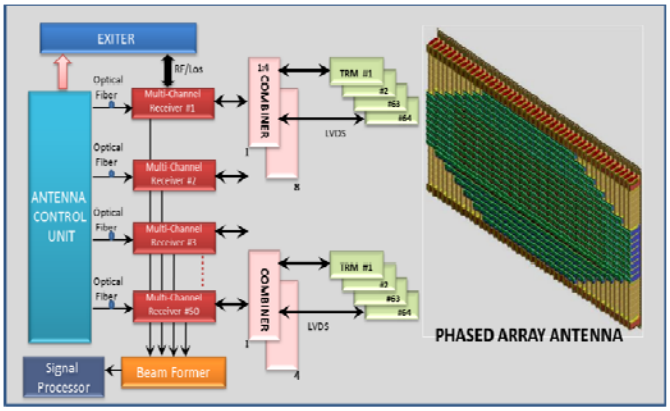

Figure 1: Context Diagram Multi Channel Receiver Configuration

IIIANALOG RECEIVER DESIGN

The Analog receiver module (ARX) of AGR houses 8 numbers of dual super heterodyne analog receiver channels[1] along with RF distribution network for LO1, LO2, IF Noise , TX drive signals and TX/BITE control circuit. ARX module receives 8 RF signals from the 8 RF I/Os of the sub arrays of Primary Radar of antenna array and are down-converted in to analog IF signals by 8 numbers of analog receiver down converter channels in receive mode. These IF outputs are further fed to DRX module for further down conversion to base band.

The ARX module also distributes amplified TX drive signal to 8 sub arrays of the Antenna array Unit. The block diagram of Analog receiver channel of ARX module is shown in the figure.2 along with 4 numbers of 1:8 power distribution networks for LO1, LO2, IF Noise and TX drive signals. Each of these Analog receiver channels should be phase and gain matched in-system through digital attenuator and phase shifter. Each of the Analog receiver channels should integrate with MSTC/RF attenuator and dynamic AGC at 2nd IF level. Each of the receiver channels should have BITE injection facility for in system receiver characterization during BITE mode along with IF O/P detector status.

Two Switchable band pass filters of different Bandwidths are employed at the final IF output stage as matched filters.

The ARX module generates the Control signals for the digital phase shifters, attenuator, Tx/BITE control circuit through FPGA[13] integrated in ARX module. This FPGA receives the control; timing signals from Digital receiver FPGA through serial/ discrete interface and sends status of ARX module to the DRX module. 8 analog receiver channels along with the RF distribution networks are appropriately housed in a single housing with proper channel to channel isolation.

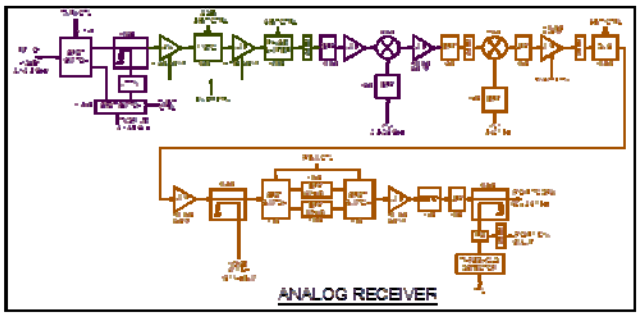

Figure 2: Architecture of Analog ReceiverUnit

The main functions of the analog receiver module are:

1. Receives and double down converts RF signal to IF signal.
2. Generating all the controls required for Transmit/ Receive, MSTC and AGC controls.
3. Amplifies and transmit during transmit mode of operation.
4. Generates required phase and attenuation values to phase shifters and attenuators during calibration and operational mode.

IVDIGITAL RECEIVER DESIGN

Digital Receiver will receives the IF signal from Analog receiver and digitalize it with the help of ADC[9]. Multi-Channel Receiver receives the message packet through the Rx FPGA interface which has in turn received the message from the DBF through the Aurora interface.

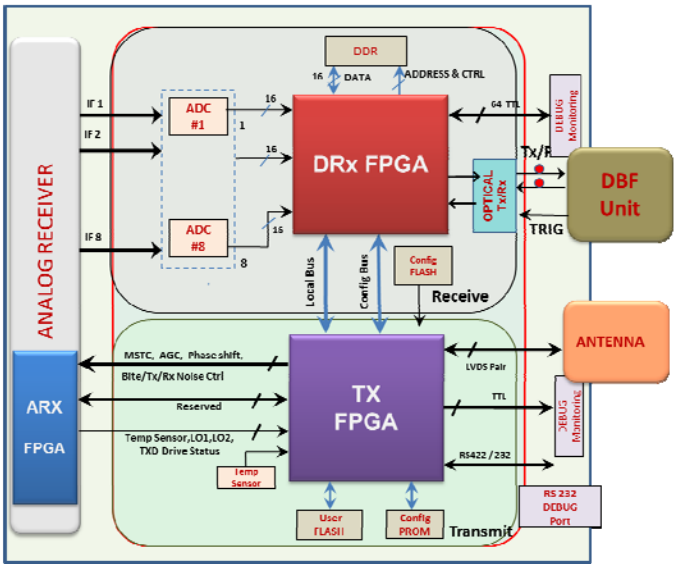

Figure 3: Architecture of Digital Receiver Unit

The Master controller reads the input command coming from the Digital Beam former validates the CSCI Destination Address and proceeds only if it is valid. It then decodes the type of command and packet size from the message header and then generates the control signals required for each of the

sub-blocks of the Multi-channel. The sub-blocks of Rx FPGA are as follows.

1. Aurora Interface and FIFO s to communicate with the DBF, through the optical channel
2. Master Controller
3. Acknowledgement Controller (ACK Controller)
4. Check sum calculators
5. ADC Interface
6. 4 ADC s, each with 2 channels
7. 8 DDC – One for each ADC channel
8. 8 FIFO's for storing ADC – IQ Data.
9. Register Interface to communicate to the register bank of Tx-FPGA
10. Flash memory Interface
11. Soft reset Module.

The main functions of the digital receiver module are:

1. FPGA based Digital Down conversion[4].
2. Generation of Radar Timing signals and controls signals for analog channels.
3. Digitizing input signal, performing Digital down conversion [9] of the signal using FPGA and then filtering out unwanted signal to generate I & Q.
4. Computation of phase and amplitude values for all the TR modules to generate Beam at desired direction.
5. Maintaining various predefined errors values and element position values.
6. Multiplexed Base Band Data transmission to DBF
7. Built in Test and status communication.

VVARIOUS OPERATIONAL MODES OF MULTI CHANNEL RECEIVER

The Multi-Channel Receiver is an important subsystem of the Radar Unit. There are 24 AGRs which are arranged in the form of a 4x6 matrix (4 Rows, 6 Columns).

This Multi-Channel unit is responsible for communicating the data from DBF to 32 DTRMs of the antenna array and effectively implementing the following modes of operations,

- Power On Self-Test - POST
- Configuration Mode –
  - Multi-Channel Receiver ID, DTRM/DRM Position & Health
- Operational Dwell Mode (Video Data Mode)
- Tx Calibration Mode
- Rx Calibration Mode
- Calibration Upload - Flashing
- Online Status Request
- Debug Mode - Online ,Offline

- Power On Self-Test (POST):

The POST operation is expected to occur soon after the Receiver is powered on. In this mode the Multi-Channel Receiver's FPGA will collect the connectivity status of the TR modules to which it is connected. It can also collect the Multi-Channel Receiver FPGA health data during this mode. This information is stored in the Flash for future use (Offline Status).

- Configuration:

There are multiple Multi Channel Receivers are present in the Antenna Array. All this receivers need to be configured with unique ID. The Configuration of each Multi-Channel Receiver is done by the DBF unit. This unit will send the configuration message in sequence to the all Muti-channel Receiver. Depending on the message the each receiver configures itself with ID. During Configuration the Master Controller configures the AGR with the AGR-ID contained in the message. This AGR-ID is used to decode the M and N values which is in turn used for calculation of phase during the Dwell operation. Also used in TX-RX calibration mode to check if the AGR is a CAL-AGR.

- Calibration:

Once the Calibration command is received, the complete responsibility of calibrating all the TRMs/RMs lies with the Multi-Channel Receiver. The message packet consists of the calibration phase and attenuation values for each TRM/RM. The receiver controller needs to sequentially enable each TRM/RM while disabling the others for one pulse of the PRT.

If the command is Tx Calibration, then the Master Controller enables the UART Controller and provides the UART Controller with the calibration values for each DTRM/DRM along with the command word for the DTRM/DRM. These values are loaded into the UART Tx Registers. Once all the values are loaded, the UART Controller then checks for the checksum error for this operation from the Master Controller. If the check sum is valid, the UART Controller transmits all the calibration values from UART Tx Registers to their respective DTRMs simultaneously.

If the command is Rx Calibration, the Master Controller still needs to enable the UART Controller and provide the command word for the DTRM/DRM along with the calibration values.

The PRT generation also happens for the Calibration mode by the PRT Generator of the timing control block based on the packet contents. During the PRT pulse ADC enables are also generated and the ACK controller packetizes the video messages and sends back with the video header information and checksum, to the DBF. Once all the 64 TRM s are calibrated, it goes back to idle state, ready to receive the new command.

During Tx calibration operation out of multiple array Receivers, one receiver will be identified CAL receiver. This CAL receiver receives while other Multi-Channel Receivers are transmitting. This CAL receiver packetizes the IQ data sent it to DBF.

During Tx calibration Multi Channel receiver will be transmitting while rx calibration NFTR probe will transmitting. The CAL line will be connected to CAL receiver one of its channels.

- Status:

Once the Status request comes from RC, the Multi-channel receiver job is to collect all status information from DTRMs.

To receive status, the multi-channel receiver sends the status request command to all 32 DTRMs or DRMs. There are 32 dedicated UARTs, which are used to receive and transmit the status or other commands to DTRMs. UART will receive one word from each of the DTRMs and store it in the register bank. Each word in the Status Register bank is read out sequentially and sent back as acknowledgement. The Multi-Channel receiver health status is also included in the response.

- Calibration Upload:

During Calibration Upload operation, the Multi-channel receiver will receive all the DTRMs calibration phase and attenuation values for all the frequency spots. These values are stored permanently into the flash memory. When we receives operational mode, the corresponding frequency's phase and attenuation values will be read from flash and stored temporarily into RAM memory.

- Debug Mode:

The Debug mode or Offline Status request comes through the RS-232 port. The Multi-Channel receiver reads status information offline through debug port.

During this mode of operation all status of DTRMs or DRM can be read. Also all other status or counter information can be read.

- Receive/Transmit Pattern Measurement Mode:

This mode used to check how the pattern will be formed during receive mode and transmit mode of operation. After receive and transmit calibration was done, calibration error values will be loaded into multi-channel receiver memory using Cal Upload mode. In pattern measurement mode the multi-channel receiver will calculate required phase values to form beam in desired direction.These calculated values of the phase and attenuation values will beadded to the cal error. UART controller picks the appropriate phase/attenuation values and sends to respective DTRMs/DRMs along with the command required by DTRM/DRM. Timing controller will generate ADC enable to ADC's and PRT to DTRMs/DRMs.

During the Receive pattern measurement the NFTR probe will transmits all the Multi-channel receiver will receives, digitalizes and packetizethe data. During the transmit pattern mode all the Multi-channel receiver will transmits NFTR probe will receives forms the beam.

VII RESULTS

All the multi-channel receivers were successfully integrated. All the radar modes of operations are synchronized with the help the SOB signal. The Multi-Channel receivers pattern was taken during receive and transmit calibration is shown in figures [4] and [5].

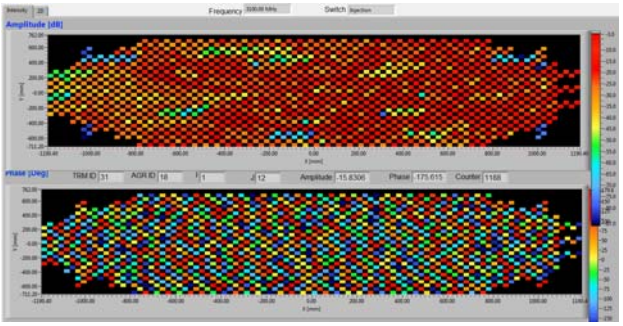

Figure 4: Multi Channel Receiver's status after RxCalibraion

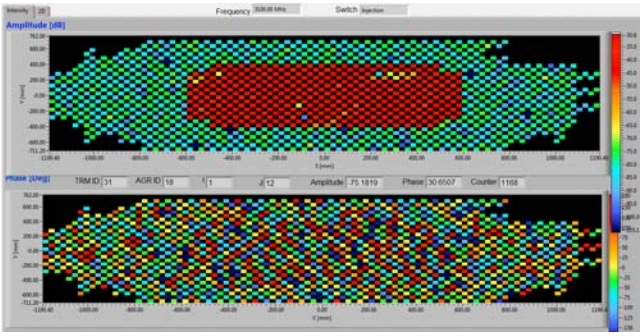

Figure 5: Multi Channel Receiver's status after Tx Calibraion

VIII CONCLUSION AND FUTURE SCOPE

The 24 no's of Multi-channel receiver units are integrated in the Antenna array. The receive and transmit paths of multi-channel receiver has been calibrated and required calibration error values are stored in each one of multi-channel receivers flash memories.These error values along actual phase and attenuation values were added. The resulted radiation pattern was measured for receive and transmit mode with the help FPGA controller logic.The hierarchical hybrid multi-channel receiver architecture design approach has given great flexibility for the radar operation and improved performance of the radar. The same FPGA Logic can be extended for any active phased arrays which consist of few thousands of Transmit and Receive modules for Beam Steering, Digital down Conversion and Digital Beam Forming.

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BIO DATA OF AUTHORS

Mr. Doddamani Govind Rao born on 2nd October 1978 at Gulbarga, Karnataka, India. He has completed his M.Tech in VLSI system Design in 2003 from NIT Warangal, Bachelor of Engineering in Electronics and Communication from Gulbarga University Gulbarga and secured 3rd rank to the University in the year 2000. He is working in LRDE, DRDO, Bangalore, India as Scientist and his areas of work include, FPGA based board design and Digital System Design.He has developed several control logics in VHDL, which has been used in the Radars. His expertise includes Digital system Design, Beam Steering and Digital Beam Forming for Active Phased array Radar.

Mr. Hassen Basha, born on 17th April 1987 at Kadapa, Andhra Pradesh. He received B.Tech Degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, in the year 2009.He is working in LRDE, DRDO as Scientist since Oct 2010. Presently he is working in the field of Array Group receiver for the development of Active Phased Array Radar. His interests include FPGA based Digital and Communication System Design.

Mr. Renuka Prasad, born on 24th June1979 at Bangalore. He obtained his B.E. in Electronics and Communication Engineering from Bapuji Institute of Engineering And Technology, Kuvempu University, Davangere, Karnataka, India in the year 2002. He is working in LRDE, DRDO as Scientist since Oct 2002. He has designed and developed Digital Radar Systems using state of art technologies. He has significantly contributed in the development of phased array antenna systems. Presently he is working in the field of Multichannel digital receiver for the development of Active Phased Array Radar. He is also involved in the area of the digital beam forming algorithms design and digital beam steering logic design for an Active Phased array Radar. His areas of interest are digital system designs for Active Array Radars, Digital T/R modules and Digital Beam forming.

Mr. Anant Raut received his B.E. degree in Electronics and Telecommunication in 2005, from SGSITS Indore, India. He worked as a lecturer in the Department of Electronics and Telecommunication of SVITS. Presently he is working as a scientist in the Electronics and Radar Development Establishment (LRDE), Bangalore. His work contributions are in the area of Active Phased Array Radar digital subsystem design and development.